AF

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	**MAIL STOP Reply Brief - Patents**
Joon-seop KWAK, et al.	Group Art Unit: 2812
Application No.: 10/673,251	Examiner: SAVITRI MULPURI
Filed: September 30, 2003	Confirmation No.: 2845
For: GaN BASED GROUP III-V NITRIDE SEMICONDUCTOR LIGHT-EMITTING DIODE AND METHOD FOR FABRICATING THE SAME	

COVER LETTER FOR COPY OF REPLY BRIEF

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

On December 13, 2007, the original Examiner's Answer was re-scanned and electronically sent to the Offices of the Undersigned. This second copy of the Examiner's Answer acknowledges Applicant's response to Notification of Non-Compliant Appeal Brief (in which the section from "V. Summary of Claims Subject Matter" was resubmitted) and acknowledges consideration of prior art cited in the Information Disclosure Statement, but otherwise does not substantively differentiate from the original Examiner's Answer.

It is not clear whether the Office is expecting a response. In case a response is necessary to return the application to the jurisdiction of the Board of Patent Appeals and

Interferences, Applicants enclose a copy of their Reply Brief and Request for Oral Hearing of October 25, 2005. Applicants did not subsequently change either the Appeal Brief or the Reply Brief.

Applicants look forward to the scheduling of an Oral Hearing, pursuant to the Request for an Oral Hearing filed October 25, 2005.

Respectfully submitted,

BUCHANAN INGERSOLL & ROONEY PC

Date: December 26, 2007 By: _____

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Patent
Attorney's Docket No. 030681-576

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REPLY BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the Examiner's Answer dated August 25, 2005, Appellants offer the following comments.

Related Proceeding Statement

At page 2 of the Examiner's Answer, the Examiner suggests that the Appeal Brief does not contain a statement regarding Related Appeals and Interferences. Appellants note page 2 of the Appeal Brief, which has this statement.

Rebuttal Regarding Kawai and Nunoue et al Patents

With respect to the Kawai patent (U.S. Patent 6,468,902), the Office suggests that the Kawai patent "substantially discloses the (sic) similar process as instant (sic) claimed process for making light emitting devices except etching the sapphire substrate by (sic) mixture of chlorine (Cl_2) (sic) and argon (Ar)." Appellants respectfully submit that this is not the case.

The Kawai patent does in fact mention Cl_2 etching in connection with removal of a GaN layer, rather than the sapphire substrate at column 10, lines 61-67. What

10-24-05

Kawai also says is, at col. 2, lines 37-44 and in particular, lines 43 and 44, that "it is actually impossible to make the via hole with any of these methods" wherein one of the methods is dry etching, e.g, with RIE. At col. 4, lines 52-53, the Kawai patent further emphasizes this point by stating the dry etching such as conventional RIE cannot be employed to make via holes. Hence, far from merely omitting a suggestion of etching through a mixture of chlorine and argon, the Kawai patent unambiguously states that forming via holes through a dry etching step is inappropriate or impossible.

At page 6 of the Examiner's Answer, the Examiner suggests that because Kawai discloses that the dry etching rate is very low, that does not mean that it is not possible to dry etch a via hole in a sapphire substrate. The Examiner further suggests that the Nunoue patent (U.S. Patent 5,905,275) teaches dry etching of a sapphire substrate. Therefore, in the Examiner's view, the Nunoue patent trumps the negative teaching of the Kawai patent in some manner. Appellants respectfully note that the Office is attempting to replace the wet etch for forming via holes in the Kawai patent with a dry etching step, whereas the Nunoue patent teaches a dry etching step for something other than via holes, *i.e.,* a large area and not a via hole that would have a high aspect ratio. Hence, as modification is suggested in the Office Action, the Kawai patent's clearly negative teaching would not be overcome by any unrelated teaching regarding the use of dry etching on sapphire substrate that do not involve via holes.

Claim 16

Appellants have placed claim 16 in independent form pursuant to 37 C.F.R. §

41.33 (b)(2) by means of a concurrently filed Amendment with Reply Brief. A new Claims Appendix is attached.

At page 8 of Appellants' Appeal Brief, Appellants mention that the hypothetical combination of references does not meet the recitations of independent method claims 1 and 23, which include a dry etching in a region of high resistant substrate using a reaction gas comprising at least Cl_2 or BCl_3 to expose the first semiconductor layer. Dependent claim 16 also recites this aspect of the invention, and the same argument applies. Accordingly, Appellants would respectfully submit that claim 16 is independently patentable from independent claim 12 by recitation of the composition of the reaction gas and have placed the claim in independent form for emphasis.

Conclusion

In light of the foregoing, and the comments made in the Appeal Brief of June 2, 2005, Appellants respectfully submit that they have pointed out errors in the Examiner's rejections including specifically identifying recitations not found in the applied art, identifying the Examiner's mischaracterizations of the references, and noting a lack of motivation to combine the references and in fact an indication that prior art would tend to teach away from a combination suggested in the Office Action.

Accordingly, Appellants respectfully request that the Examiner's rejections be overturned and the application returned to the Examiner for prompt allowance.

Respectfully submitted,

BUCHANAN INGERSOLL PC

Date: October 25, 2005

By: _____
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CLAIMS APPENDIX

Claim 1: A method for fabricating a light-emitting device, the method comprising:

(a) sequentially forming a first compound semiconductor layer, an active layer, and a second compound semiconductor layer, which are for inducing light emission, on a high-resistant substrate;

(b) forming a light-transmitting conductive layer on the second compound semiconductor layer;

(c) dry etching a region of the high-resistant substrate using a reaction gas comprising at least Cl_2 or BCl_3 to expose the first compound semiconductor layer; and

(d) forming a light-shielding conductive layer to cover the exposed region of the first compound semiconductor layer.

Claim 2: The method of claim 1, wherein step (c) comprises:

polishing the bottom of the high-substrate; and

exposing the bottom of the first compound semiconductor layer by etching the region of the high-resistant substrate.

Claim 3: The method of claim 2, wherein the high-resistant substrate is a sapphire substrate.

Claim 4: The method of claim 2, wherein the bottom of the high-resistant substrate is polished by grinding or lapping.

Claim 5 (canceled).

Claim 6: The method of claim 1, wherein the reactant gas further comprises Ar gas.

Claim 7-8 (canceled).

Claim 9: The method of claim 2, wherein the high-resistant substrate is etched to form a via hole through which the bottom of the first compound semiconductor layer is exposed.

Claim 10: The method of claim 2, wherein the high-resistant substrate is etched to expose a portion of the bottom of the first compound semiconductor layer that is larger than a portion of the first compound semiconductor layer that remains in contact with the high-resistant substrate after etching.

Claim 11: The method of claim 1, further comprising forming a pad layer on the light-transmitting conductive layer.

Claim 12: A method for fabricating a light-emitting device, the method comprising:

(a) sequentially forming a first compound semiconductor layer, an active layer, and a second compound semiconductor layer, which are for inducing light emission, on a high-resistant substrate;

(b) forming a light-reflecting conductive layer on the second compound semiconductor layer;

(c) etching a region of the high-resistant substrate to expose the first compound semiconductor layer; and

(d) forming a light-transmitting conductive layer to cover the exposed region of the first compound semiconductor layer.

Claim 13: The method of claim 12, wherein step (c) comprises:

polishing the bottom of the high-resistant substrate; and

exposing the bottom of the first compound semiconductor layer by etching the region of the high-resistant substrate.

Claim 14: The method of claim 13, wherein the high-resistant substrate is a sapphire substrate.

Claim 15: The method of claim 13, wherein the bottom of the high-resistant substrate is polished by grinding or lapping.

Claim 16: A method for fabricating a light-emitting device, the method comprising:

(a) sequentially forming a first compound semiconductor layer, an active layer, and a second compound semiconductor layer, which are for inducing light emission, on a high-resistant substrate;

(b) forming a light-reflecting conductive layer on the second compound semiconductor layer;

(c) etching a region of the high-resistant substrate to expose the first compound semiconductor layer; and

(d) forming a light-transmitting conductive layer to cover the exposed region of the first compound semiconductor layer,

wherein the high-resistant substrate is dry etched using a reaction gas comprising at least Cl_2 or BCl_3.

Claim 17: The method of claim 16, wherein the reactant gas further comprises Ar gas.

Claim 18: The method of claim 13, wherein the high-resistant substrate is dry etched using a reaction gas comprising at least Cl_2 or BCl_3.

Claim 19: The method of claim 18, wherein the reactant gas further comprises Ar gas.

Claim 20: The method of claim 13, wherein the high-resistant substrate is etched to form a via hole through which the bottom of the first compound semiconductor layer is exposed.

Claim 21: The method of claim 13, wherein the high-resistant substrate is etched to expose a portion of the bottom of the first compound semiconductor layer that is larger than a portion of the first compound semiconductor layer that remains in contact with the high-resistant substrate after etching.

Claim 22: The method of claim 12, further comprising forming a pad layer on the light-transmitting conductive layer.

Claim 23: A method for fabricating a light-emitting device, the method comprising:

(a) forming a material layer for lasing on a high-resistant substrate;

(b) forming a first electrode on the material layer;

(c) dry etching a region of the high-resistant substrate using a reaction gas comprising at least Cl_2 or BCl_3 to expose a region of the material layer; and

(d) forming a second electrode on the bottom of the high-resistant substrate to cover partially or fully the exposed region of the material layer.

Claim 24: The method of claim 23, wherein step (a) comprises:

sequentially forming a first compound semiconductor layer, a first cladding layer, a resonator layer, a second cladding layer, and a second compound semiconductor layer on the high-resistant substrate;

forming a mask pattern on the second compound semiconductor layer to cover a predetermined region of the second compound semiconductor layer;

sequentially patterning the second compound semiconductor layer and the second cladding layer using the mask pattern as an etch mask, the second cladding layer into a rigid form;

removing the mask pattern; and

forming a passivation layer on the second cladding layer patterned into the ridge form, in contact with a region of the patterned second compound semiconductor layer.

Claim 25: The method of claim 24, wherein step (c) comprises:

polishing the bottom of the high-resistant substrate; and

exposing the bottom of the first compound semiconductor layer by etching the region of the high-resistant substrate.

Claim 26: The method of claim 25, wherein the high-resistant substrate is a sapphire substrate.

Claim 27: The method of claim 25, wherein the bottom of the high-resistant substrate is polished by grinding or lapping.

Claim 28-30 (canceled).

Claim 31: The method of claim 24, wherein the reactant gas further comprises Ar gas.

Claim 32: The method of claim 25, wherein the high-resistant substrate is etched to form a via hole through which the bottom of the first compound semiconductor layer is exposed.

Claim 33: The method of claim 25, wherein the high-resistant substrate is etched to expose a portion of the bottom of the first compound semiconductor layer that is larger than a portion of the first compound semiconductor layer that remains in contact with the high-resistant substrate after etching.

Claim 34: The method of claim 24, wherein the resonator layer is formed by sequentially forming a first waveguide layer, an active layer, and a second waveguide layer on the first cladding layer.

Claim 35: The method of claim 23, wherein step (d) comprises:

forming an ohmic contact layer on the bottom of the high-resistant substrate to cover partially or fully the exposed region of the material layer; and

forming a thermal conductive layer on the ohmic contact layer.